Amendments to the Specification

Please add the following replacement paragraphs for paragraphs [0028] and [0029]:

[0028] During operation a gate bias V_g is applied to gate electrode 51 and a drain voltage V_d is applied to drain electrode 66 while the source electrode is grounded. When the gate bias V_g exceeds the threshold voltages of device 10 (i.e., gate voltages necessary to form channel regions ~~47,~~ 57, 571, 572, 573, and 58), current components I_1, I_2, I_3, and I_4 flow between source region 43 and trench drain region 36.

[0029] One advantage of the present invention is that n-type regions 16, 18, and 21 provide additional low resistance paths or drift regions for current to flow, which reduces on resistance R_{ON}, without increasing the area of device 10. This reduces R_{ON}*Area without detrimentally impacting the blocking voltage of device 10 or increasing die or chip size. When under a positive gate bias, gate trench portion 47 causes electrons to accumulate at the interface between layers 16, 18, and 21 and gate trench portion ~~46~~ 47 thereby further reducing the resistance in the areas.